among the electrical contact points of the top metallization structure is smaller than the number of electrical contact points of the interconnecting metallization structure by a measurable amount.

PLEASE AMEND THE CLAIMS AS FOLLOWS:

29. A semiconductor device structure comprising:

a semiconductor substrate comprising semiconductor devices;

an interconnecting metallization structure comprising lower metal lines, connected to said devices;

electrical contact points on an upper surface of said interconnecting metallization structure and connected to said interconnecting metallization structure;

a passivation layer deposited over said interconnecting metallization structure and over said electrical contact points;

openings through said passivation layer, exposing said electrical contact points; and

C 6 cont

an upper metallization structure within said openings and over said passivation layer, comprising upper metal lines, connected to said interconnecting metallization structure , wherein said upper metal lines are substantially thicker than said lower metal lines.

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30. The structure of claim 29 wherein the upper metallization structure connects portions of said interconnecting metallization structure to other portions of said interconnecting metallization structure.

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31. The structure of claim 29 wherein said upper metallization structure comprises:

a plurality of insulating layers;

one or more of said upper metal lines formed between said insulating layers; and

a plurality of contact pads in an upper layer of said metallization structure, connected to one or more of said upper metal lines.

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32. The structure of claim 31 wherein said upper metal lines comprise lines that are selected from the group consisting of signal lines, power buses and ground buses, or a combination thereof, and wherein said upper metal lines are

substantially wider than said lower metal lines in said interconnecting metallization structure.

Please cancel claims 33-37

38. The structure of claim 29 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um, wherein said contact points comprise tungsten, copper (electroplated or electroless), aluminum, or polysilicon, .

39. The structure of claim 29 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0 um Plasma Enhanced CVD (PECVD) oxide over which a layer within the range of approximately 0.5 to 2.0 um PECVD nitride is deposited.

40. The structure of claim 29 further comprising an insulating, separating layer formed over said passivation layer, wherein said insulating, separating layer is a polymer..

41. The structure of claim 40 wherein said insulating, separating layer comprises polyimide.

42. The structure of claim 40 wherein said insulating, separating layer comprises the polymer benzocyclobutene (BCB).

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43. The structure of claim 40 wherein said insulating layer is of a thickness after curing within the range of approximately 1.0 to 30 um.

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44. The structure of claim 29 wherein said openings have an aspect ratio within the range of approximately 1 to 10.

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45. The structure of claim 29 wherein said upper metallization system is formed to provide fan-out capability, wherein a distance separating contact points in a top layer of said upper metallization structure is greater than a distance separating electrical contact points in said interconnecting metallization structure.

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46. The structure of claim 29 wherein said the number of said electrical contact points in said upper metallization structure is larger than the number of said electrical contact points of said interconnecting metallization structure, by a substantial amount.

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47. The structure of claim 29 wherein said upper metallization system is formed to provide relocation capability, wherein electrical contact points in a top layer of said upper metallization system are connected to electrical contact points in said interconnecting metallization structure, wherein said relocation capability is provided by providing said electrical contact points in said top layer of said upper

metallization system in s different sequence than said electrical contact points in said interconnecting metallization structure.

C7 cont 15 48. The structure of claim 29 wherein said upper metallization structure is formed to provide reduction capability, wherein electrical contact points in a top layer of said upper metallization structure are connected to electrical contact points, which are functionally equivalent to each other, in said interconnecting metallization structure, whereby the number of said electrical contact points in said upper metallization structure is less than the number of electrical contact points in said interconnecting metallization structure.

PLEASE ADD THE FOLLOWING NEW CLAIMS:

C8 16 80. The structure of Claim 31 wherein said insulating layers in said upper metallization structure comprise an organic material, wherein said insulating layers are thicker than intermetal dielectric layers in said interconnecting metallization structure.

17 81. The structure of Claim 80 wherein said intermetal dielectric layers in said interconnecting metallization structure for formed of an inorganic material.

18 82. The structure of Claim 29 wherein openings between said upper metal lines are wider than openings formed between said lower metal lines.

83. The structure of Claim 29 wherein said top metallization structure provides a means to standardize next level packaging.

84. The structure of Claim 83 wherein said next level packaging is Ball Grid Array (BGA) packaging.

85. The structure of Claim 29 wherein said top metallization structure provides a means to simplify next level packaging.

86. The structure of Claim 29 further comprising solder balls on pads on a top layer of said top metallization structure, for connection to next level packaging.

87. The structure of Claim 29 further comprising wires bonded to pads on a top layer of said top metallization structure, for connection to next level packaging.

88. A semiconductor device structure comprising:

a semiconductor substrate comprising semiconductor devices;

an interconnecting metallization structure comprising lower metal lines, connected to said devices;

electrical contact points on an upper surface of said interconnecting metallization structure and connected to said interconnecting metallization structure;

a passivation layer deposited over said interconnecting metallization structure and over said electrical contact points;

openings through said passivation layer, exposing said electrical contact points; and

an upper metallization structure within said openings and over said passivation layer, comprising upper metal lines, connected to said interconnecting metallization structure, wherein said upper metal lines are substantially wider than said lower metal lines.

89. A semiconductor device structure comprising:

a semiconductor substrate comprising semiconductor devices;

an interconnecting metallization structure comprising lower metal lines in layers, separated by inorganic intermetal dielectric layers, connected to said devices;

electrical contact points on an upper surface of said interconnecting metallization structure and connected to said interconnecting metallization structure;

a passivation layer deposited over said interconnecting metallization structure and over said electrical contact points;

openings through said passivation layer, exposing said electrical contact points; and

an upper metallization structure within said openings and over said passivation layer, comprising upper metal lines, separated by organic dielectric layers, connected to said interconnecting metallization structure, wherein said organic dielectric layers are thicker than said inorganic intermetal dielectric layers.

90. A semiconductor wafer, comprising:

a semiconductor substrate having an upper passivation layer, through which contact pads are exposed, wherein semiconductor devices are formed on said semiconductor substrate, an interconnecting metallization structure comprising lower metal lines being connected to said devices; and

an upper metallization structure over said passivation layer, connected to said contact pads, comprising upper metal lines, in one or more layers, wherein said upper metal lines are substantially wider than said lower metal lines.

91. The semiconductor wafer of Claim 90, wherein said one or more layers of upper metal lines are separated by organic dielectric layers.

92. The semiconductor wafer of Claim 90, wherein upper contact pads are formed in a top layer of said one or more layers of said upper metal lines.

93. The semiconductor wafer of Claim 92 wherein solder bumps are formed on said upper contact pads.

94. The semiconductor wafer of Claim 90, wherein said upper metallization structure is configured to provide fan-out, relocation and reduction capabilities.

95. A semiconductor wafer, comprising:

a semiconductor substrate having an upper passivation layer, through which contact pads are exposed, wherein semiconductor devices are formed on said semiconductor substrate, an interconnecting metallization structure comprising lower metal lines being connected to said devices; and

an upper metallization structure over said passivation layer, connected to said contact pads, comprising upper metal lines, in one or more layers, wherein said upper metal lines are substantially thicker than said lower metal lines.